

REMARKS/ARGUMENTS

I. STATUS OF CLAIMS

Claims 1-6, 9-15 and 17 are pending.

Claim 9 has been amended to include the subject matter of claim 17, and thus, claim 17 has been cancelled without prejudice. It is respectfully submitted that no new matter has been added and that all claims are fully supported by the specification.

Claims 1-6 and 9-15 are presented for examination.

II. Claim Rejections under 35 U.S.C. § 103(a)

Claims 1-6, 9-15 and 17 stand rejected under 35 U.S.C. § 103(c) as allegedly being anticipated by Mates (U.S. Patent No. 6,564,347). The applicants respectfully traverse the rejection for the following reasons.

Claim 1 is directed towards an integrated circuit that includes, among other features, *an internal memory containing test routines that the processing core executes to test the integrated circuit, wherein the internal memory contains a first set of test routines for execution during a production test of the integrated circuit and a second set of test routines for execution during an in-product test of the integrated circuit.*

The Examiner alleges that Mates' on-chip logic analyzer unit LAU 105 included in the integrated circuit 100 discloses the claimed recitations. Specifically, the Examiner cites the following from Mates (col. 7, lines 54-60) to allege that Mates discloses the claimed first set of test routines for execution during a production test:

"Using embedded LAUs in integrated circuits in accordance with the invention, integrated circuit manufacturers and testers may be able to realize significant savings related to test equipment by obviating a need for costly, external logic analyzers. As a need for external logic analyzers is reduced, so are the costs associated with maintenance, repair, etc."

In the above cited paragraph, Mates does not disclose a test routine for execution during a *production test*. Instead, Mates merely discloses that by using the embedded LAU, the IC manufacturers may be able to realize significant savings. The applicants respectfully point out that the mere mention of an IC manufacturer (in relation

with potential cost saving using the embedded LAU) does not imply that Mates discloses, or even suggests that the LAU 105 includes a test routine for execution during a *production test*, as is recited in claim 1. Instead, Mates simply refers to a cost savings because the embedded LAU 105 eliminates the need for an external logic analyzer to test the integrated circuit.

Additionally, the LAU 105 of Mates is shown in a computer system 200 in Fig. 2, which includes several components in addition to the host IC 100 (which includes the LAU 105), e.g., input devices 215, output devices 210, bus 205, data storage medium 235, etc. While explaining the operation of the LAU 105, Mates discloses the following:

In operation, a user may initiate a test of the host integrated circuit chip 100 by the LAU 105 via the input device(s) 215 of the computer system 200. Such an input signal may be received by the LAU 105 via the bus 205 and the host I/O circuitry 120... (Mates, col. 5, lines 9-13).

The response vector(s) may be displayed to a user via the output device(s) 210 and/or stored in the LAU response vector storage memory 170. If the response vector(s) are displayed, they may be communicated from the chip 100 to the output device(s) 210 via the host I/O circuitry 120 and the bus 205... (Mates, col. 5, lines 49-53).

A test program that makes use of on-chip LAU test capabilities may be downloaded over a network to a system including the host integrated circuit chip and stored in, for example, the data storage medium 235 of FIG. 2.... (Mates, col. 8, lines 1-5)

Thus, while explaining the operation of the LAU 105, Mates discloses initiating the tests by input devices 215 via bus 205, outputting the responses through output devices 210, storing test programs in the data storage medium 235, etc. The input devices 215, output devices 210, bus 205, data storage medium 235, etc. are not a part of the LAU 105; rather, these are parts of the computer system 200 of Fig. 2. Hence, Mates discloses the operation of the LAU 105 while the LAU 105 and the host IC 100 is already included in the computer system 200. That is, Mates does not disclose, or even suggest the test routines of the LAU 105 executing during a *production test*, as would

be required by claim 1. Rather, Mates discloses using the LAU when it is already inside the computer system 200, i.e., while it is inside the intended product.

For at least these reasons, the applicants respectfully submit that Mates does not disclose or even suggest the recited first set of test routines for execution during a *production test* of the integrated circuit. Rather, Mates' LAU 105's operation is akin to the recited second set of test routines for execution during an *in-product test* of the integrated circuit. Accordingly, it is respectfully submitted that claim 1 is allowable along with associated dependent claims 2-6.

Independent claim 9 has been amended to include features from now cancelled claim 17. Claim 9 is now directed towards a method that includes, among other features, *when the control signal has a first state, the test routines selected implement a production test of the integrated circuit; and when the control signal has a second state, the test routines selected implement a system-level test of the integrated circuit.* For at least the reasons discussed with respect to claim 1, it is respectfully submitted that Mates does not disclose or even suggest such a method and therefore, does not anticipate claim 9. Accordingly, claim 18 is allowable, along with associated dependent claims 10-15.

Conclusion

For these reasons, a Notice of Allowance is respectfully requested. Please contact the undersigned at (503) 796-2997 regarding any questions or concerns associated with the present matter. If any fees are due in connection with this paper, the Commissioner is authorized to charge Deposit Account 500393.

Respectfully submitted,
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